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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CALLAHAN, PAUL E	
ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/818,425	GENTILE, ROBERT	
	Examiner	Art Unit	
	Paul Callahan	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *45-55* is/are allowed.

6)☐ Claim(s) *1-13,16-25,28,29 and 36-44* is/are rejected.

7)☒ Claim(s) *14,15,26,27 and 30-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 1-59 are pending in this application and have been examined.

Drawings

2. The drawings submitted 2-9-2005 are objected to because they are not marked as "Replacement Sheets" as per 37 CFR 1.121.

Response to Arguments

3. Applicant's arguments filed 2-9-2005 have been fully considered but they are not persuasive.

The Applicant argues that the applied references may be distinguished from the claimed invention since the password area and data file area of Junya et al. "do not have the same structure/functionality as the applicant's check register. However the Examiner counters that the features of Junya do read on the applicant's check register within a reasonably broad interpretation of that term. The access permission signal generated by the storage device of Junya upon comparison of the password read out of the register reads on the applicant's write-enable signal.

The Applicant argues that the Davis '981 patent fails to teach what type of access to the BIOS is permitted. Yet it is inherent to the system of Davis that such access would include control of write operations to the memory for updating the BIOS.

The Applicant asserts that Davis does not teach does not teach the generation or disablement of any type of signal that controls access to the BIOS. Yet such is indeed taught at col. 4 lines 34-37.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, and 36 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Junya, US 5,469,564.

As for claim 1, Junya teaches a flash memory device comprising: a memory array; and a check register to store an access code (fig. 1 items 15, 16), wherein the check register generates a write enable signal to the memory array in response to the access code (col. 1 lines 39-62).

As or claim 2, Junya teaches a flash memory device wherein the check register toggles a write enable signal in response to an externally provided access code (col. 1, lines 55-62).

As for claim 36, Junya teaches a processor system comprising: a non-volatile memory device (fig. 1 item 10); a code register coupled to the non-volatile memory device (fig. 1 item 15); and a processor coupled to provide a request code to the code register fig. 1 item 11), wherein the code register controls a write enable signal of the non-volatile memory device (fig. 1 item 13, col. 2 lines 32-47).

As for claim 37, Junya teaches a processor system wherein the code register is volatile (abstract, col. 1 lines 39-61).

6. Claims 56-59 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Davis US 6,633,981.

As for claim 56, Davis '981 teaches a method of operating a memory system comprising: generating an enable code (col. 5 lines 5-35); issuing a write request from a processor (col. 5 lines 9-14), the write request comprises a request code (col. 5 lines 9-14); and comparing the request code to the enable code and providing a write enable signal to a memory device in response to the comparison (col. 5 lines 18-22).

As for claim 57, Davis '981 teaches a method of claim 56 wherein the enable code is generated by the processor (col. 5 lines 21-24).

As for claim 58, Davis '981 teaches a method wherein a processor generates the enable code while executing a BIOS program during an initialization operation of the processor (col. 4 lines 62-67, col. 5 lines 1-15)

As for claim 59, Davis '981 teaches a method of claim wherein the BIOS program is stored in a memory (fig. 2 item 220)

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6-11, 13, 16-25, 27-29, and 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis, US 5,844,986, Davis, US 6,633,981 and Official Notice taken as detailed below.

As for claim 6, Davis '981 teaches a memory system comprising: a memory array having a BIOS program stored therein (abstract, fig. 4), wherein the BIOS program contains a program to generate a random access code when executed by a processor (col. 5 lines 5-15); and a check register to store the random access code (col. 5 lines 5-15), wherein the check register enables write operations (generates a write enable

signal) to the memory array based upon an externally provided access code (fig. 4, col. 5 lines 15-25). Davis does '981 does not teach a BIOS memory that is a flash memory. However Davis '986 does teach this feature (fig. 1 item 42). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '986 into the system of Davis 981. The motive to make this combination is the ability of such flash memory to resist attack by computer viruses. This is discussed for example, as a concern in col. 1, lines 39-47 of Davis '981, and as a solution to that shortcoming in the prior art, in Davis '986 col. 1 lines 26-45.

As for claim 7, Davis teaches a memory system of wherein the BIOS program directs the processor to write the random access code to the check register to enable write operations in response to an external write request (col. 5 lines 5-41).

As for claim 8, Davis '981 a flash memory system where the program to generate the access code is located in a portion of the flash memory array that is protected from being written over (fig. 5 item 220).

As for claim 9, Davis '981 teaches a flash memory system wherein the check register further comprises: a compare register to store codes; an access code register to store the random access code; and a register control circuit to compare a code stored in the compare register to the random access code (col. 5 lines 5-42) wherein the register control circuit enables write operations (generates a write enable signal) when a

code written to the compare register matches the random access code (col. 4 lines 23-45).

As for claim 10, Davis teaches a flash memory system of claim 9 wherein the first write of a code to the compare register after boot up is stored in the access code register (col. 4 lines 60-67, col. 5 lines 1-5).

As for claim 11, Davis '981 teaches a memory system comprising: a processor to process data (fig. 2 item 210); a memory array storing a BIOS program to instruct the processor to generate an access code (fig. 2 item 220); and a check register to store the access code generated by the processor (fig. 2 item 220), wherein the check register enables write operations (generates a write enable signal) to the memory array in response to writes of the access code (col. 5 lines 5-30). Davis does '981 does not teach a BIOS memory that is a flash memory. However Davis '986 does teach this feature (fig. 1 item 42). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '986 into the system of Davis 981. The motive to make this combination is the ability of such flash memory to resist attack by computer viruses. This is discussed as a concern in col. 1 lines 39-47 of Davis '981, and as a solution to that shortcoming in the prior art, in Davis '986 col. 1 lines 26-45.

As for claim 13, Davis teaches a flash memory system wherein the BIOS program controls writes of the access code to the check register (col. 5 lines 1-15).

As for claim 16, Davis teaches a flash memory system comprising: a processor to process data (fig. 2 item 210); a memory array storing a BIOS program (fig. 2 item 220), the BIOS program containing a program to instruct the processor to generate an access code at power up (col. 4 lines 65-67, col. 5 lines 1-15); control circuitry to control write operations to the memory array in response to a write enable signal (col. 5 lines 5-30); and a check register to store the access code generated by the processor (col. 5 lines 15-20), wherein the check register toggles the write enable signal in response to writes of the access code (col. 5 lines 20-30).

As for claim 17, Davis teaches a flash memory system wherein the first write to the check register of the access code sets the access code in the check register (col. 5 lines 20-30).

As for claim 18, Davis '981 teaches a memory system wherein a request for access to the memory array must contain an authorization code that is recognized by the BIOS program (col. 5 lines 15-25). Davis '981 does not however teach a write operation request as the memory access request. However Davis '986 does teach such a write request directed at access to BIOS stored in flash memory (col. 1 lines 25-45). Therefore it would have been obvious to one of ordinary skill in the art at the time of the

invention to incorporate this feature into the system of Davis '981. Motive to make the combination is found in Davis '981 (col. 1 lines 39-63) and Davis '986 (col. 1 lines 25-45) where the desirability of authentication control over access to BIOS stored in memory, Flash Memory in the case of Davis '986, is discussed.

As for claim 19, the combination of Davis '981 and Davis '986 does not teach a flash memory system of where in a write enable signal is toggled between an inactive HIGH signal and an active LOW signal. However Official Notice may be taken that the use of such logical states in analog and digital control circuitry is a step that is old and well known in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature into the system of Davis '981 and Davis '986. It would have been desirable to do so as this would allow for simple and low cost control of read / write operations to BIOS memory.

As for claim 20, the combination of Davis '981 and Davis '986 does not teach a flash memory system further comprising: a logic circuit to supply an inactive HIGH write enable signal to the control circuitry upon completion of a write operation to the memory array. However Official Notice may be taken that the use of such logical states in analog and digital control circuitry is a step that is old and well known in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature into the system of Davis '981 and Davis '986. It would have

been desirable to do so as this would allow for simple and low cost control of read / write operations to BIOS memory.

As for claim 21, the combination of Davis '981 and Davis '986 does not teach a flash memory system wherein the write enable signal is toggled between an inactive LOW signal and an active HIGH signal. However Official Notice may be taken that the use of such logical states in analog and digital control circuitry is a step that is old and well known in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature into the system of Davis '981 and Davis '986. It would have been desirable to do so as this would allow for simple and low cost control of read / write operations to BIOS memory.

As for claim 22, the combination of Davis '981 and Davis '986 does not teach a flash memory system further comprising: a logic circuit to supply an inactive LOW write enable signal to the control circuitry upon completion of a write operation to the memory array. However Official Notice may be taken that the use of such logical states in analog and digital control circuitry is a step that is old and well known in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature into the system of Davis '981 and Davis '986. It would have been desirable to do so as this would allow for simple and low cost control of read / write operations to BIOS memory.

As for claim 23, Davis '981 teaches a system comprising: a memory array having a BIOS program (fig. 2 item 220); a processor to execute the BIOS program (fig. 2 item 220); control circuitry to control write operations to the memory array in response to a write enable signal (fig 2 item 220, 230, fig. 1 item 105); and a check register to store a random access code generated by the BIOS program (fig. 2 item 220), wherein the check register gates the write enable signal to the control circuitry in response to the random access code (col. 5 lines 5-30). Davis does '981 does not teach a BIOS memory that is a flash memory. However Davis '986 does teach this feature (fig. 1 item 42). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '986 into the system of Davis 981. The motive to make this combination is the ability of such flash memory to resist attack by computer viruses. This is discussed as a concern in col. 1 lines 39-47 of Davis '981, and as a solution to that shortcoming in the prior art, in Davis '986 col. 1 lines 26-45.

As for claim 24, the combination of Davis '981 and Davis '986 does not teach a flash memory device wherein the random access code is stored in volatile memory so the random access code is erased when power is removed from the check register. However Official Notice may be taken that such a feature is old and well known in the art of anti-tampering secure memory. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature into the system of Davis '981 and Davis '986. It would have been desirable to do so as a means of thwarting any attempt to remove and tamper with the BIOS flash memory controlling

authentication operations. Motive to make this combination is found in Davis '981 (col. 1 lines 38-62) where "battery-backed" memory independent of the operating system is advocated as a basis for authentication operations.

As for claim 25, Davis '981 teaches a memory system wherein the memory array and the check register are embedded in a single memory. Davis '981 does not teach the use of flash memory. However Davis '986 does teach this feature (fig. 1 item 42). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '986 into the system of Davis 981. The motive to make this combination is the ability of such flash memory to resist attack by computer viruses. This is discussed as a concern in col. 1 lines 39-47 of Davis '981, and as a solution to that shortcoming in the prior art, in Davis '986 col. 1 lines 26-45.

As for claim 28, Davis '981 teaches a memory system comprising: a memory array having a BIOS program stored therein (fig. 2 item 220); control circuitry to control write operations to the memory array (col. 5 lines 5-30); a processor to execute the BIOS program (fig. 1 item 105); and a program logic device to store a random access code generated by the processor from instructions contained in the BIOS program, wherein the program logic device gates a write enable signal to the control circuitry in response to the random access code (col. 5 lines 5-35). Davis '981 does not teach the use of flash memory. However Davis '986 does teach this feature (fig. 1 item 42). Therefore it would have been obvious to one of ordinary skill in the art at the time of the

invention to incorporate this feature of Davis '986 into the system of Davis 981. The motive to make this combination is the ability of such flash memory to resist attack by computer viruses. This is discussed as a concern in col. 1 lines 39-47 of Davis '981, and as a solution to that shortcoming in the prior art, in Davis '986 col. 1 lines 26-45.

As for claim 29, Davis '981 teaches a memory system of claim 28 wherein the random access code is specific to each boot cycle (col. 4 lines 62-67, col. 5 lines 1-15).

As for claim 42, Davis '981 teaches a method of operating a memory comprising: generating a random access code at power up (col. 5 lines 5-35); writing the access code to a check register (col. 5 lines 5-35); and toggling write enable signals in response to writes of the access code to the check register (col. 5 lines 20-25). Davis '981 does not teach a memory that is a flash memory. However Davis '986 does teach this feature (fig. 1 item 42). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '986 into the system of Davis 981. The motive to make this combination is the ability of such flash memory to be field erasable ("battery-backed"): This is discussed as a concern in col. 1 lines 39-47 of Davis '981 where the ability to remove and compromise non-volatile memory is discussed.

As for claim 43, Davis '981 teaches a BIOS program stored in memory that instructs a processor to generate the access code (col. 5 lines 5-30). Davis '981 does

not teach a memory that is a flash memory. However Davis '986 does teach this feature (fig. 1 item 42). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '986 into the system of Davis 981. The motive to make this combination is the ability of such flash memory to be field erasable ("battery-backed"). This is discussed as a concern in col. 1 lines 39-47 of Davis '981 where the ability to remove and compromise non-volatile memory is discussed.

As for claim 44, Davis '981 teaches a BIOS program that controls the writes of the access code to the check register (col. 5 lines 5-30).

9. Claims 3-5 and 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Junya as applied to claims 1 and 36, Davis '981, and Official Notice taken as detailed below.

As for claim 3, Junya teaches all of the limitations of claim 1 upon which claim 3 depends, but does not teach a flash memory device wherein a check register is volatile so the access code is erased when power is removed from the check register. Davis '981 does teach such an erasable memory (col. 1 lines 38-62: "battery backed"). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature into the system of Junya. It would have been desirable to do so as a countermeasure to removal and tampering with the flash

memory. Motive to make this combination is found for example in Junya col. 1 lines 13-35 where the need for a system to prevent tampering with memory is detailed.

As for claim 4, Junya does not teach a memory device wherein the access code is randomly generated by a program executed by a processor. However Davis '981 does teach such a feature (col. 5 lines 5-3). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '981 into the system of Junya. It would have been desirable to do so as this would allow for more robust challenge response protocols to be undertaken between a user seeking access to a secure memory and a processor controlling access. Motive to make this combination is found for example, in col. 1 lines 20-35, where Junya describes how simple password protections are easily defeated.

As for claim 5, does not teach a flash memory device wherein the program is generally executed immediately after power is applied to the processor. However Davis '981 does teach such a feature (col. 4 lines 62 through col. 5 lines 15). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '981 into the system of Junya. The motive to make this combination is found for example, in Junya in col. 1 lines 20-35, where Junya describes how simple password protection schemes for system memory are easily defeated.

As for claim 38, Junya teaches all the limitations of claim 36, but does not teach a processor that generates an enable code and programs the enable code in the code register. However Davis '981 does teach such a feature (col. 5 lines 5-3). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '981 into the system of Junya. It would have been desirable to do so as this would allow for more robust challenge response protocols to be undertaken between a user seeking access to a secure memory and a processor controlling access. Motive to make this combination is found in col. 1 lines 20-35 where Junya describes how simple password protections are easily defeated.

As for claim 39, Junya teaches a processor system wherein the code register compares the request code to the enable code to control the write enable signal (col. 2 lines 34-45).

As for claim 40, Junya does not teach a processor wherein the processor generates the enable code while executing a basic input/output program (BIOS). However Davis '981 does teach this feature (col. 5 lines 62-67, col. 5 lines 1-23). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '981 into the system of Junya. Motive to make the combination may by found in col. 1 lines 38-47 of Davis '981 where the desirability of preventing corruption to BIOS memory during boot up is described.

As for claim 41, Junya does not teach a processor wherein BIOS is stored in non-volatile memory. Davis '981 does teach this feature (fig. 2 items 240, 220). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Davis '981 into the system of Junya. The motive to make the combination is found in col. 1 lines 38-47 of Davis '981 where the ability of non-volatile BIOS memory to resist attack during boot up is described.

Allowable Subject Matter

10. Claims 45-55 are allowed.

11. Claims 14, 15, 26, 27, and 30-35 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following US Patent document detail memory protection systems similar to that of the applicant.

Helbig 6,311,273

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Callahan whose telephone number is (703) 305-1336. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Andrew Caldwell, can be reached on (703) 306-3036. The fax phone number for the organization where this application or proceeding is assigned is: (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Andrew Caldwell

6/9/05

Paul Callahan

ANDREW CALDWELL
SUPERVISORY PATENT EXAMINER